FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **MAT-8097US**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/786524

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/04476	**6 Jul 2000 (.06.07.00)**	**7 Jul 1999 (07.07.99)**

TITLE OF INVENTION
REPRODUCED SIGNAL PROCESSOR

APPLICANT(S) FOR DO/EO/US
Masatoshi Taniguchi; Takeshi Otsuka; Nobukatsu Okuda; Hirofumi Uchida; Shinya Tanaka

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)). (UNEXECUTED)
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

English translation of PCT/ISA/210

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/786524	PCT/JP00/04476	MAT-8097US

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$970.00	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$840.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$690.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$670.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$96.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =		$860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		$0.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	11 - 20 =	0	x $18.00	$0.00	
Independent claims	3 - 3 =	0	x $78.00	$0.00	
Multiple Dependent Claims **(check if applicable)**.			☐	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$860.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**.			☐	$0.00	
SUBTOTAL =				$860.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	$0.00	
TOTAL NATIONAL FEE =				$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	$0.00	
TOTAL FEES ENCLOSED =				$860.00	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **18-0350** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Lawrence E. Ashery
Ratner & Prestia
P.O. Box 980
Valley Forge, PA 19482
Tel: (610) 407-0700

SIGNATURE

Lawrence E. Ashery
NAME

34,515
REGISTRATION NUMBER

March 6, 2001
DATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	M. Taniguchi et al.	: Art Unit:
Serial No.:	To Be Assigned	: Examiner:
Filed:	Herewith	:
FOR:	REPRODUCED SIGNAL PROCESSOR	:

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231
S I R :

Prior to examination, please amend the above application as follows:

IN THE SPECIFICATION:

After the title and before the first paragraph, please insert the following paragraph:

THIS APPLICATION IS A U.S. NATIONAL PHASE APPLICATION OF PCT INTERNATIONAL APPLICATION PCT/JP00/04476.

IN THE DRAWINGS:

Please delete page "17/17" of the drawings, also labeled as "LIST OF REFERENCE NUMERALS" in its entirety.

IN THE CLAIMS:

Please replace claim 4 with the following amended claim:

4. (As Amended) The reproduced signal processing apparatus of claim 2, wherein said transmitting means transmits the information showing whether n pieces of frame data to be transmitted are valid or invalid, by adding to the transmission data.

Please replace claim 7 with the following amended claim:

7. (As Amended) The reproduced signal processing apparatus of claim 5, wherein said transmitting means transmits the information showing whether two pieces of frame data to be transmitted are valid or invalid, by adding to the data.

Please add the following new claims:

10. (Newly Added) The reproduced signal processing apparatus of claim 3, wherein said transmitting means transmits the information showing whether n pieces of frame data to be transmitted are valid or invalid, by adding to the transmission data.

11. (Newly Added) The reproduced signal processing apparatus of claim 6, wherein said transmitting means transmits the information showing whether two pieces of frame data to be transmitted are valid or invalid, by adding to the data.

Respectfully submitted,

Lawrence E. Ashery, Reg. No. 34,515
Attorney for Applicants

LEA/lm
Enclosure: Version With Markings Showing Changes Made
Dated: March 6, 2001
Suite 301, One Westlakes, Berwyn
P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

EXPRESS MAIL Mailing Label Number: EL769591258US
Date of Deposit: March 6, 2001

I hereby certify that this paper and fee are being deposited, under 37 C.F.R. § 1.10 and with sufficient postage, using the "Express Mail Post Office to Addressee" service of the United States Postal Service on the date indicated above and that the deposit is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Kathleen Libby
Kathleen Libby

VERSION WITH MARKINGS SHOWING CHANGES MADE

SPECIFICATION:

After the title and before the first paragraph:

THIS APPLICATION IS A U.S. NATIONAL PHASE APPLICATION OF PCT INTERNATIONAL APPLICATION PCT/JP00/04476.

CLAIMS:

4. (As Amended) The reproduced signal processing apparatus of claim 2 ~~or 3~~, wherein said transmitting means transmits the information showing whether n pieces of frame data to be transmitted are valid or invalid, by adding to the transmission data.

7. (As Amended) The reproduced signal processing apparatus of claim 5 ~~or 6~~, wherein said transmitting means transmits the information showing whether two pieces of frame data to be transmitted are valid or invalid, by adding to the data.

Claim 10 has been added.

Claim 11 has been added.

DESCRIPTION

Reproduced signal processor

TECHNICAL FIELD

The present invention relates to a reproduced signal processing apparatus for processing data reproduced at an arbitrary speed from a recording medium in which data is recorded in sync block units together with identification information of sync blocks.

BACKGROUND ART

In a helical scanning VCR, a prior art about double speed reproduction and shuttle reproduction by so-called non-tracking method is disclosed, for example, in Japanese Laid-open Patent No. 9-139019.

This prior art discloses the following.

(1) In 2-speed or 4-speed reproduction, reproduced data of two frames or four frames are issued by decimating one frame.

(2) In up to 1-speed drive, data of one frame is transmitted, in 2-speed drive, two frames are transmitted, and in 4-speed drive, four frames are transmitted. Composition of data in transmission is arranged in the recording order, and quantity of data corresponding to the speed is transmitted.

In this prior art, however, the following problems are known.

(1) Since transmission data does not include all of reproduced data, a reproduced image of smooth motion cannot be obtained from transmission data at an arbitrary speed.

(2) It is hard to arrange the data in the recording order at an arbitrary reproduction speed. That is, it is hard to transmit data reproduced at an arbitrary reproduction

speed.

SUMMARY OF THE INVENTION

To solve these problems, a reproduced signal processing apparatus of the invention comprises sync block detecting means for detecting identification information of reproduced data, data information generating means for generating data information composed of track information, field information and frame information from the identification information, first memory means for storing plural frames of reproduced data, memory writing means for writing reproduced data in the first memory means on the basis of the identification information, memory reading means for reading out parallel the data of n frames (n being an integer of 2 or more satisfying the relation of $\alpha \leqq n$) accumulated in the first memory means, and transmitting means for transmitting n pieces of transmission data by restructuring or without restructuring n pieces of frame data being read out by the memory reading means on the basis of the data information.

A reproduced signal processing apparatus in other example of the invention comprises sync block detecting means for detecting identification information of reproduced data, data information generating means for generating data information composed of track information, field information and frame information from the identification information, first memory means for storing plural frames of reproduced data, memory writing means for writing reproduced data in the first memory means on the basis of the identification information, memory reading means for reading out parallel the data of n frames (n being an integer of 2 or more satisfying the relation of $\alpha \leqq n$) accumulated in the first memory means, and reproduction output control means.

It further comprises (1) delay means for issuing data of

n frames being read out by the memory reading means by delaying by one field and two fields each, and also issuing data of n-th frame by delaying by three fields, and reproduction output control means for selecting and issuing outputs of the delay means and memory reading means in field units on the basis of the data information. Or it also comprises (2) second memory means for accumulating data of n frames being read out by the memory reading means for the portion of three frames each, and reproduction output control means for selecting and issuing field data on the basis of the data information, from the data delayed by one frame and two frames by controlling the second memory means.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration of a reproduced signal processing apparatus in embodiment 1 of the invention.

Fig. 2 is a flowchart showing a generation algorithm of track information in embodiment 1.

Fig. 3 is a flowchart showing a generation algorithm of field information in embodiment 1.

Fig. 4 is a flowchart showing a generation algorithm of frame information in embodiment 1.

Fig. 5 is a timing chart for generating data information in the case of $\alpha = 0.9$ in embodiment 1.

Fig. 6 is a timing chart of data information and frame data being read out by a memory reading circuit in embodiment 1.

Fig. 7 is a timing chart for restructuring data in the case of $\alpha = 0.9$ in embodiment 1.

Fig. 8 is a timing chart for restructuring data in the case of $\alpha = 1.5$ in embodiment 1.

Fig. 9 is a block diagram showing a configuration of a

reproduced signal processing apparatus in embodiment 2 of the invention.

Fig. 10 is an operation explanatory diagram of output control in embodiment 2.

Fig. 11 is a timing chart of field regeneration in embodiment 2.

Fig. 12 is a block diagram showing a configuration of a reproduced signal processing apparatus in embodiment 3 of the invention.

Fig. 13 is an operation explanatory diagram of output control in embodiment 3.

Fig. 14 is a timing chart of field regeneration in the case of $\alpha = 1.5$ in embodiment 3.

Fig. 15 is a block diagram showing a configuration of a reproduced signal processing apparatus in embodiment 4 of the invention.

Fig. 16 is a timing chart for restructuring data in the case of $\alpha = 3.0$ in embodiment 4.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring now to the drawings, preferred embodiments of the invention are described below.

(Embodiment 1)

Fig. 1 is a block diagram showing a configuration of a reproduced signal processing apparatus in embodiment 1 of the invention. This embodiment is designed to transmit data reproduced at an arbitrary α-times speed (an integer satisfying the relation of $\alpha \leqq n$) in a range of standard reproducing speed ± 2 times ($n = 2$).

In Fig. 1, reproduced data 100 is data reproduced at arbitrary α-times speed within ± 2 times speed by so-called non-tracking method. Or the reproduced data 100 may be once recorded in a disk device and reproduced from the disk

device. The reproduced data 100 is provided with identification information of sync block in sync block units of specified length.

A sync block detecting circuit 101 detects a sync signal of reproduced data 100, and detects and issues identification information 102. The identification information 102 is composed of sync block number and track number. The track number is also a unit in encoding time of outer correction code.

After the sync signal is detected, the data is put into an inner correction circuit 103 to undergo inner error correction. A memory writing circuit 104 determines the data writing address by using the identification data 102, and accumulates the data corrected of inner error into a first memory 105.

A data information generating circuit 106 issues data information 108 showing the status of accumulation in the memory 105 from the identification information 102. The data information 108 is composed of track information, field information, and frame information.

<Generation of track information>

Generation of track information is determined on the basis of the track number. However, the reproduced data 100 is not always the tracked data, and different track numbers may be reproduced consecutively. Therefore, when the track number of the identification information 102 is used directly as the track information, it cannot be judged accurately which track number the data accumulated in the memory 105 has.

Accordingly, the track number detected finally in the time required to reproduce one track number in 1-speed reproduction (hereinafter called head switch time) is compared with the track information of one head switch time before.

In the case there are two kinds of track numbers to be reproduced continuously in non-tracking state, and in the case of forward direction reproduction (+ reproduction), the track

information is the value of subtracting the correction value 2 from the last track number detected in the head switch time.

The reason why the correction value is 2 is, in the case of reproduction of two kinds of track numbers in one head switch time, that the data having these track numbers is not completely accumulated yet, and that the data of the track having the number two places away from the present track number is completely accumulated.

Accordingly, the track information of one head switch time before, and the value subtracting correction value 2 from the last track number detected in the head switch time are compared, and the larger value is updated as new track information.

In the case of backward direction reproduction (- reproduction), the track information of one head switch time before, and the value adding correction value 2 to the last track number detected in the head switch time are compared, and the smaller value is updated as new track information.

Referring now to Fig. 2, an algorithm of generating track information by the data information generating circuit 106 is explained.

At step 200, the identification information 102 detected by the sync block detecting circuit 101 is latched in the last place of head switch time. That is, a track number (TN) is latched.

At step 201, depending on the data reproducing direction, the latched track number is corrected as follows, and a corrected track number (CTN) is generated.

(1) In the case of positive direction reproduction

Corrected track number = track number - 2 (correction value)

However, when track number is 1, correction track number is 9, and when track number is 2, correction track

number is 10.

(2) In the case of negative direction reproduction

Corrected track number = track number + 2 (correction value)

However, when track number is 9, correction track number is 1, and when track number is 10, correction track number is 2.

At step 202, the corrected track number and the track information of data information 108 of one head switch time before are compared as follows.

(1) In the case of positive direction reproduction

When corrected track number is 1 or 2,

(corrected track number + 10) > track information of one frame before

Or when corrected track number is 2 to 10,

corrected track number > track information of one frame before

When this condition is established, the process goes to step 203, and the corrected track number is updated as track information.

If not established, the process goes to step 200 without updating the track information.

(2) In the case of negative direction reproduction

When corrected track number is 1 to 8,

corrected track number < track information of one frame before

Or when corrected track number is 9 or 10,

corrected track number < (track information of one frame before + 10)

When this condition is established, the process goes to step 203, and the corrected track number is updated as track information.

If not established, the process goes to step 200 without

updating the track information.

<Generation of field information>

Field information is generated from the track information according to the algorithm in Fig. 3. When data of one frame is recorded in 10 tracks (track numbers 1 to 10), in positive direction reproduction, in track information from 1 to 5, data in the first half field of one frame is being accumulated. In track information from 6 to 10, data in latter half field is being accumulated. The field information is supposed to be at low level while accumulating data in first half field, and at high level while accumulating data in latter half field.

Referring to Fig. 3, an algorithm of generating field information of data information 108 by the data information generating circuit 106 is explained.

At step 300, track information of data information 108 is monitored.

At step 301, it is judged whether the monitored track information is a value of 1 to 5, or a value of 6 to 10.

(1) In positive direction reproduction, when the track information is 1 to 5, or in negative direction reproduction, when the track information is 6 to 10, the process goes to step 302, and the field information is set to low level.

(2) In positive direction reproduction, when the track information is 6 to 10, or in negative direction reproduction, when the track information is 1 to 5, the process goes to step 303, and the field information is set to high level.

In this algorithm, data of one frame is recorded in 10 tracks, but it can be processed similarly in the case of 12, 20 or other tracks.

<Generation of frame information>

Frame information is generated according to an algorithm shown in Fig. 4, by judging whether data of n frames

is accumulated or not in the memory 105, from the field information.

Referring to Fig. 4, the algorithm of generating frame information by the data information generating circuit 106 is explained.

At step 400, field information of data information 108 is monitored. It is monitored whether the field information is promoted by one period or not, that is, changed from high to low.

At step 401, when it is judged that the field information is promoted by one period, the frame information is counted up at step 402. When this count value is n, it is reset to 0.

As a result, the frame information shows a value of 0 to n-1.

If it is not judged that the field information is promoted by one period, back to step 400, monitoring of field information is continued.

Fig. 5 is a timing chart for generating data information in the case of $\alpha = 0.9$ in embodiment 1.

In Fig. 5, (a) is a signal showing head switching time (Tsw), (b) denotes a track number of identification information 102, (c) denotes track information of data information 108, (d) denotes field information of data information 108, and (e) denotes frame information of data information 108.

Alphanumeric symbols in Fig. 5 (b), (c) indicate track numbers, and "a" means that the track number is 10. In Fig. 5 (e), the numeral refers to the value of frame information.

The track number is detected, for example, in every sync block, and it may change from an intermediate point in relation to head scanning to the tracks.

In the case of $\alpha = 0.9$, while reproducing data of one frame, at least one track number may be reproduced in different head switch times. In Fig. 5 (b), track numbers 8

and 9 are issued in different head switch times. As a result, the track information, field information, and frame information are changed.

Consequently, the data accumulated in the memory 105 is corrected in the outer correction circuit 107. The data to be corrected is determined by the track information. Later, when outer corrected data are accumulated in the memory 105 for two frames, the memory reading circuit 109 can read out data of two new frames.

Whether data of two frames is accumulated or not is judged on the basis of the change of frame information of data information 108. The data to be read out is changed over in synchronism with a next frame signal when the frame information in data information 108 shows that data for two frames is accumulated. Of the data being read out in two frames, the reproduction time is earlier in data 110, and later in data 111.

Fig. 6 is a timing chart of data information and frame data being read out by the memory reading circuit in embodiment 1.

In Fig. 6, (a) is a reproduction reference frame signal, (b) is reproduced data 100 to be entered in the sync block detecting circuit 102, (c) is frame information of data information 108, (d) is frame data 110 being read out by the memory reading circuit 109, and (e) is frame data 111 being read out by the memory reading circuit 109.

Alphabetic letters in Fig. 6 (b), (d), (e) are symbols attached to frames, and the alphabetic order is the sequence being recorded in the VCR.

The data of two frames 110, 110 thus being read out are restructured into main data and sub data on the basis of the field information and frame information of the data information 108 in a transmitting circuit 112. The main data

is sent out to a transmission output terminal 113, and sub data is sent out to a terminal 114, and transmitted. The transmitting circuit 112 restructures, if only main data is transmitted, so that much of frame data in the data reproduced at α-times may be transmitted.

When α is less than 1.0, it is restructured so that frame data 110 or 111 may be transmitted as main data. Data is restructured, in one frame period of reproduction reference frame signal, on the basis of two-bit value composed of field information of the data information 108 as LSB and frame information as MSB, and its change.

When the two-bit value changes as follows, the frame data 110 is issued as both main and sub data. At this time, the sub data is same as the main data, and is hence provided with a flag showing invalid data.

(1) When not changed as 0 or 1

(2) When changed from 3 to 0

(3) When changed from 0 to 1

(4) When changed from 2 to 3, and to 0

(5) When changed from 3 to 0, and to 1

Or when changed follows, the frame data 111 is issued as both main and sub data. At this time, the sub data is same as the main data, and is hence provided with a flag showing invalid data.

(6) When not changed as 2 or 3

(7) When changed from 1 to 2

(8) When changed from 2 to 3

(9) When changed from 0 to 1, and to 2

(10) When changed from 1 to 2, and to 3

Fig. 7 is a timing chart showing data restructuring in the case of α = 0.9 in embodiment 1.

In Fig. 7, (a) is a reproduction reference frame signal, (b) is field information of data information, (c) is frame

information of data information, (d) is frame data 110, (e) is frame data 111, (f) is output data from a main data output terminal 113, and (g) is output data from a sub data output terminal 114.

In addition to data structuring when $\alpha = 0.9$, Fig. 8 shows a timing chart showing data restructuring in the case of $\alpha = 1.5$ in embodiment 1. When α is larger than 1.0, aside from the case of $\alpha \leqq 1.0$ mentioned above, the two-bit value changes as follows.

(11) When changed sequentially from 0 to 1, 2, and 3, the frame data 111 is issued as both main data and sub data.

In this case, too, the sub data is same as the main data, and is hence provided with a flag showing invalid data.

(12) When changed sequentially from 1 to 2, 3, and 0, the frame data 110 is issued as both main data and sub data.

In this case, too, the sub data is same as the main data, and is hence provided with a flag showing invalid data.

(13) When changed sequentially from 2 to 3, 0, and 1; or

(14) When changed sequentially from 3 to 0, 1, and 2

The frame data 110 is issued to the main data transmission terminal 113, and the frame data 111 to the sub data transmission terminal 114. Herein, the main data and sub data are different, and are both provided with a flag showing valid data.

In this manner, all of the data reproduced at an ordinary speed α within ± 2 times can be transmitted without changing the transmission rate. Or by transmitting the main data only, much of reproduced data can be transmitted.

That is, from the state of change of field information (one bit) and frame information (n types, for example, one bit if n = 2), the data accumulation status can be judged, and the accumulation can be predicted. In synchronism with the

reproduction reference frame signal, the frame data to be issued (that can be issued) is judged. Hence, data can be restructured so as to transmit all data at α-times speed.

In embodiment 1, the case of n = 2 is explained, but if n = 4, 8 or other integer larger than 2, the transmission data can be restructured by extending the same concept.

(Embodiment 2)

Fig. 9 is a block diagram showing a configuration of a reproduced signal processing apparatus in embodiment 2 of the invention. In this embodiment, n is 2, and the same reference numerals as in Fig. 1 are not explained herein.

The reproduction operation of the reproduced signal processing apparatus of the embodiment is explained. It is same as in embodiment 1 from input of reproduced data 100 until the memory reading circuit 109 reads out data of two frames.

Of the data of two frames being read out by the memory reading circuit 109, earlier data 110 and later data 111 of reproduction time being read out are fed into a delay circuit 900.

The delay circuit 900 is composed of FIFO 901, 902, 903, 904, and 905 for delaying data by one frame. The data 110 is fed into the FIFO 901, and the output of the FIFO 901 is fed into the FIFO 902. The data 111 is fed into the FIFO 903, and its output is fed into the FIFO 904. The output of the FIFO 904 is fed into the FIFO 905.

A reproduction output control circuit 913 has input terminals S1, S2, S3, S4, S5, S6, and S7. The data 110 issued from the memory reading circuit is fed into the terminal S3. The output data from the FIFO 901 and FIFO 902 are fed into the terminals S2 and S1, respectively. The data 111 issued from the memory reading circuit is fed into the terminal S7. The output data from the FIFO 903, FIFO 904, and FIFO 905

are fed into the terminals S6, S5, and S4, respectively.

The reproduction output control circuit 913 selects the data entered in the terminals S1 to S7 by using the field information and frame information of the data information 108, and issues to an output terminal 914.

The reproduction output control circuit 913 selects the data to be issued on the basis of data information (DIm-1) in the closest reproduction reference frame period (Tm-1) and data information (DIm-2) in frame period (Tm-2) of one frame earlier. More specifically, on the basis of the two-bit value composed of field information of data information as LSB and frame information as MSB, the data to be issued is selected according to (1) the initial two-bit value (initial value) in the reproduction reference frame period, and (2) the number of times of changes of two-bit value in this period or in the first half and second half of the period.

That is, the data is selected as shown in Fig. 10. For example, (1) if the number of times of changes of two-bit value in Tm-1 is 1, the change position is in the first half field, and the initial value is 0, and (2) if the number of times of change in Tm-2 is 0 and the initial value is 0, the data fed in the terminal S1 is selected in the first half field, and the data fed in the terminal S3 in the second half.

For example, the timing chart when reproduced at α = 1.5 according to Fig. 10 is shown in Fig. 11. Fig. 11 is a timing chart of field reproduction in embodiment 2.

In Fig. 11, (a) is a reproduction reference frame signal, (b) is field information of data information 108, (c) is frame information of data information 108, (d) is result of change of data information 108 in the closest frame period (Tm-1), (e) is result of change of data information 108 in the period (Tm-2) of one frame earlier, (f) is frame data 110, and (g) is frame data 111. Further, (h) denotes an input terminal of the

reproduction output control circuit 913 for selecting according to Fig. 10 on the basis of (d) and (e), and (i) is video data issued from a video output terminal 914.

In Fig. 11 (d) and (e), for example, "0-3" indicates that the state of field information and frame information of data information starts from 0 (initial value) at the beginning of one frame, and shows the number of times of change in one frame is 3. Further, in (i), for example, "c-1" indicates the first field (first half of the field) of frame data c, and if "1" is replaced by "2", it means the second field (second half of the field).

In this way, by restructuring the data reproduced at an arbitrary speed α within ± 2 times, field slow reproduction and field double speed reproduction of smooth motion are realized.

In embodiment 2, the case of n = 2 is explained, but if n = 4, 8 or other integer larger than 2, smooth field reproduction is possible by extending the same concept. Or the field output may be also selected in a different manner from the case of Fig. 10.

(Embodiment 3)

Fig. 12 is a block diagram showing a configuration of a reproduced signal processing apparatus in embodiment 3 of the invention. In this embodiment, n is 2, and the same reference numerals as in Fig. 1 are not explained herein.

The reproduction operation of the reproduced signal processing apparatus of the embodiment is explained. It is same as in embodiment 1 from input of reproduced data 100 until the memory reading circuit 109 reads out data of two frames.

Of the data of two frames being read out by the memory reading circuit 109, data 110 being read out earlier in reproduction time is written into a memory 1101, and data 111

being read out later is written into a memory 1102. The memories 1101 and 1102 compose a second memory 1100. The memories 1101 and 1102 have a capacity of storing data of at least three frames. They are mapped so as to be written into an independent region in each frame. Writing into the memories 1101, 1102 is controlled by an upper bit address signal 1104 in each frame of reproduction reference frame in the region of the memory map, and the entered frame data is delayed by two frames. For example, when the memories 1101, 1102 have a capacity of storing data of three frames, they are mapped so that the upper two bits of the memory address may indicate three regions of the memory.

A reproduction output control circuit 1103 controls to issue data from which field by using the field information and frame information of data information 108, and reads out data from the memory 1100, and issues to a video output terminal 1106 in the field unit.

The reproduction output control circuit 1103, same as the control circuit 913 explained in embodiment 2, controls data reading from the memory 1100 on the basis of the data information. That is, the reproduction output control circuit 1103 selects the data to be issued on the basis of data information (DIm-2) in frame period (Tm-2) of one frame earlier than the closest reproduction reference frame period (Tm-1) and data information (DIm-3) in frame period (Tm-3) of one more frame earlier .

More specifically, on the basis of the two-bit value composed of field information of data information as LSB and frame information as MSB, data reading from the memory 1100 is controlled according to (1) the initial two-bit value (initial value) in the reproduction reference frame period, and (2) the number of times of changes of two-bit value in this period or in the first half and second half of the period. The reason of

using the data information of one frame earlier and two frames earlier is that it takes one frame time to write data into the memory 1100. Specific control of data reading from the memory 1100 is conducted as shown in Fig. 13.

For example, in "F1-1, S2-1" in Fig. 13, "F1-1" indicates the field data to be read out from the memory 1100 in the first half field time of the reproduction reference frame, and "S2-1" denotes the field data to be read out in the second half field time. Further, "F" shows the output from the memory 1101, and "S" is the output from the memory 1102. Numerals 1 and 2 following F and S indicate data delayed by one frame and two frames, respectively. Numerals 1 and 2 following the hyphen (-) indicate the first half field and second half field, respectively.

For example, in embodiment 3 in Fig. 13, the timing chart of field reproduction at $\alpha = 1.5$ is shown in Fig. 14.

In Fig. 14, (a) is a reproduction reference frame signal, (b) is field information of data information 108, (c) is frame information of data information 108, (d) is result of change of data information 108 of one frame earlier, (e) is result of change of data information 108 of two frames earlier, (f) is frame data 110, and (g) is frame data 111, (h) is one-frame delay data of the memory 1101, (i) is two-frame delay data of the memory 1101, (j) is one-frame delay data of the memory 1102, and (k) is two-frame delay data of the memory 1102. Further, (l) is delay data to be read out by the reproduction output control circuit 1103 according to Fig. 13 on the basis of (d) and (e), and (m) is video data issued from a video output terminal 1106.

In Fig. 14 (d) and (e), for example, "1-3" indicates that the number of times of change is 1 and the initial value is 3.

In this way, by restructuring the data reproduced at an arbitrary speed α within ± 2 times, field slow reproduction

and field double speed reproduction of smooth motion are realized.

In embodiment 3, the case of n = 2 is explained, but if n = 4, 8 or other integer larger than 2, smooth field reproduction is possible by extending the same concept. Or the manner of reading out from the reproduction output control circuit 1103 is not limited to the method shown in Fig. 13.

(Embodiment 4)

Fig. 15 is a block diagram showing a configuration of a reproduced signal processing apparatus in embodiment 4 of the invention. In this embodiment, n is 4, and the same reference numerals as in Fig. 1 and Fig. 12 are not explained herein.

The reproduction operation of the reproduced signal processing apparatus of the embodiment is explained. It is same as in embodiment 3 from input of reproduced data 100 until the memory reading circuit 109 reads out data of four frames, and stores in the memory 1100.

The memory 1100 is composed of four memories 1107, 1108, 1109, and 1110. When data of four frames are accumulated in the memory 105, the memory reading circuit 109 in the embodiment issues the oldest frame data 1500 in reproduction time, second oldest frame data 1501, third oldest frame data 1502, and the latest frame data 1503 in reproduction time.

Four frame data 1500, 1501, 1502, and 1503 being read out from the memory reading circuit 109 are delayed by one frame and two frames in the memories 1107, 1108, 1109, and 1110.

A transmission circuit 1504 reads out one or two frame data from eight pieces of delayed data on the basis of the field information and frame information of the data information 108.

In this embodiment, two frame data 1505 and 1506 are read out, and restructured, and transmitted from two transmission output terminals 1507 and 1508.

Restructuring is conducted by extending the concept of embodiment 3, on the basis of change of three bits, using two bits composed of field information of the data information 108 at LSB and frame information at MSB side. In embodiment 3, the field to be reproduced and issued is determined on the basis of the change of the data information 108, whereas the frame data including the field to be issued is read out in this embodiment.

Fig. 16 shows a timing chart of restructuring by the transmitting circuit 1504 at $\alpha = 3$.

In Fig. 16, (a) is a reproduction reference frame signal, (b) is three-bit data information (frame information: 2 bits, field information: 1 bit), (c) is result of observation of change of data information 108 of one frame earlier (Tm-1), (d) is result of observation of change of data information 108 of two frames earlier (Tm-2), (e) is frame data 1500, (f) is frame data 1501, (g) is frame data 1502, and (h) is frame data 1503. Further, (i) and (j) are delayed frame data 1505 and 1506 to be read out from the memory 1100 on the basis of (c) and (d) by the transmission circuit 1504, (k) is field data to be read out from the memory 1100 in the case of field reproduction output, (l) is actual field data in the case of field reproduction output, (m) is output data from a main data transmission output terminal 1507, and (n) is output data from a sub data transmission output terminal 1508.

In Fig. 16 (i), (j), (k), A is the data delayed by memory 1107, B by memory 1108, C by memory 1109, and D by memory 1110. For example, "1" of "A1" means data delayed by one frame, or "2" is data delayed by two frames. In (k), "1" following the hyphen (-) indicates the first field (first half

field) and "2" is the second field (second half field). In Fig. 16 (c) and (d), "3" of "3-6" means that the state of field information and frame information of data information starts from 3 (initial value) at the beginning of one frame, and "6" means it is changed six times in one frame (number of changes).

In this way, by restructuring the data reproduced at an arbitrary speed α within ± 4 times into data of two frames and transmitting, the transmission rate is small, and field slow reproduction and field double speed reproduction of smooth motion at the reception side are realized. Or if other than n = 4, by restructuring into data of two frames and transmitting, similarly, field slow reproduction and field double speed reproduction of smooth motion at the reception side are realized.

INDUSTRIAL APPLICABILITY

According to the reproduced signal processing apparatus of the invention, by restructuring the data reproduced at an arbitrary speed α within $\pm$ n times depending on the accumulation status (reproduction status) in the memory, all reproduced data can be transmitted. Further, by adequately changing over and controlling the reproduced data at an arbitrary speed α within $\pm$n times depending on the accumulation status (reproduction status), field slow reproduction and field double speed reproduction of smooth motion are realized. Moreover, by restructuring the data reproduced at an arbitrary speed α within $\pm$ n times depending on the accumulation status (reproduction status), without transmitting all the reproduced data, field slow reproduction and field double speed reproduction of smooth motion at the reception side are realized.

CLAIMS

1. A reproduced signal processing apparatus, being an apparatus for processing data reproduced from a recording medium in which data is recorded in sync block units together with the identification information of sync block, at a speed of $\pm\alpha$ times (α being an integer) of usual reproducing speed, comprising:

sync block detecting means for detecting the identification information of the reproduced data,

data information generating means for generating data information composed of track information, field information and frame information from the identification information,

first memory means for storing plural frames of the reproduced data,

memory writing means for writing reproduced data in said first memory means on the basis of the identification information,

memory reading means for reading out parallel the data of n frames (n being an integer of 2 or more satisfying the relation of $\alpha \leqq n$) accumulated in said first memory means, and

transmitting means for transmitting n pieces of transmission data by restructuring or without restructuring n pieces of frame data being read out by said memory reading means on the basis of the data information.

2. The reproduced signal processing apparatus of claim 1, wherein said transmitting means either transmits n pieces of frame data being read out by said memory reading means without restructuring, or transmits n pieces of transmission data restructured by selecting m pieces out of n pieces (m being an integer satisfying the relation of $m < n$), according to the data information.

3. The reproduced signal processing apparatus of

claim 2, wherein said transmitting means, transmitting one of n pieces of transmission data as main data and others as sub data, can transmit many frame data of data reproduced at α times as main data, and also restructures so as to transmit all frame data reproduced at α times by transmitting all of main data and sub data.

4. The reproduced signal processing apparatus of claim 2 or 3, wherein said transmitting means transmits the information showing whether n pieces of frame data to be transmitted are valid or invalid, by adding to the transmission data.

5. The reproduced signal processing apparatus of claim 1, wherein said transmitting means further comprises second memory means for accumulating n pieces of frame data being read out by said memory reading means for the portion of three frames, and

m pieces (m being 1 or 2) of frame data are read out on the basis of the data information, from the data delayed by one frame and two frames, by controlling said second memory, and are restructured into two pieces of transmission data.

6. The reproduced signal processing apparatus of claim 5, wherein said transmitting means restructures the data delayed by one frame and two frames so as to obtain reproduction output of α times at the reception side.

7. The reproduced signal processing apparatus of claim 5 or 6, wherein said transmitting means transmits the information showing whether two pieces of frame data to be transmitted are valid or invalid, by adding to the data.

8. A reproduced signal processing apparatus, being an apparatus for processing data reproduced from a recording medium in which data is recorded in sync block units together with the identification information of sync block, at a speed of $\pm\alpha$ times (α being an integer) of usual reproducing speed,

comprising:

sync block detecting means for detecting the identification information of the reproduced data,

data information generating means for generating data information composed of track information, field information and frame information from the identification information,

first memory means for storing plural frames of the reproduced data,

memory writing means for writing the reproduced data in said first memory means on the basis of the identification information,

memory reading means for reading out parallel the data of n frames (n being an integer of 2 or more satisfying the relation of $\alpha \leqq n$) accumulated in said first memory means,

delay means for issuing n pieces of frame data being read out by said memory reading means by delaying by one field and two fields each, and also issuing data of n-th frame by delaying by three fields, and

reproduction output control means for selecting and issuing outputs of said delay means and memory reading means in field units on the basis of the data information.

9. A reproduced signal processing apparatus, being an apparatus for processing data reproduced from a recording medium in which data is recorded in sync block units together with the identification information of sync block, at a speed of $\pm\alpha$ times (α being an integer) of usual reproducing speed, comprising:

sync block detecting means for detecting the identification information of the reproduced data,

data information generating means for generating data information composed of track information, field information and frame information from the identification information,

first memory means for storing plural frames of the

reproduced data,

memory writing means for writing the reproduced data in said first memory means on the basis of the identification information,

memory reading means for reading out parallel the data of n frames (n being an integer of 2 or more satisfying the relation of $\alpha \leqq n$) accumulated in said first memory means,

second memory means for accumulating n pieces of frame data being read out by said memory reading means for the portion of three frames each, and

reproduction output control means for selecting and issuing field data on the basis of the data information, from the data delayed by one frame and two frames by controlling said second memory means.

(57) **Abstract:** A reproduced signal processor comprising sync block detecting means (100), data information generating means (106), first memory means (105), memory writing means (104), memory reading means (109) for parallel reading data of n frames (n is an integer of 2 or more satisfying α<n) stored in the first memory means (105), and transferring means (112, 1504) for transferring n pieces of transfer data after restructuring n pieces of frame data read out by the memory reading means (109) according to the data information or not restructuring them.

Fig. 1

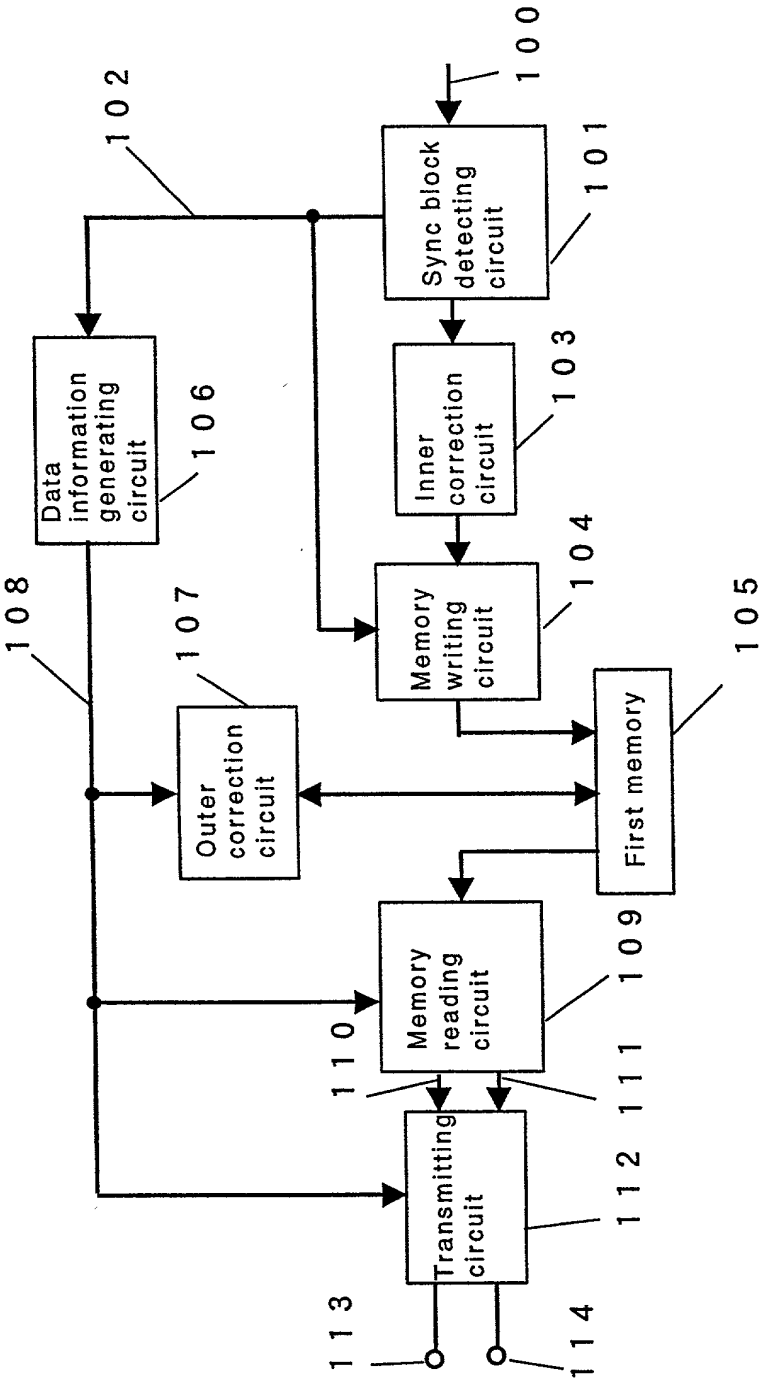

100
102
Sync block detecting circuit
101
Data information generating circuit
106
Inner correction circuit
103
Memory writing circuit
104
105
108
107
Outer correction circuit
First memory
Memory reading circuit
109
110
111
112
Transmitting circuit
113
114

Fig. 2

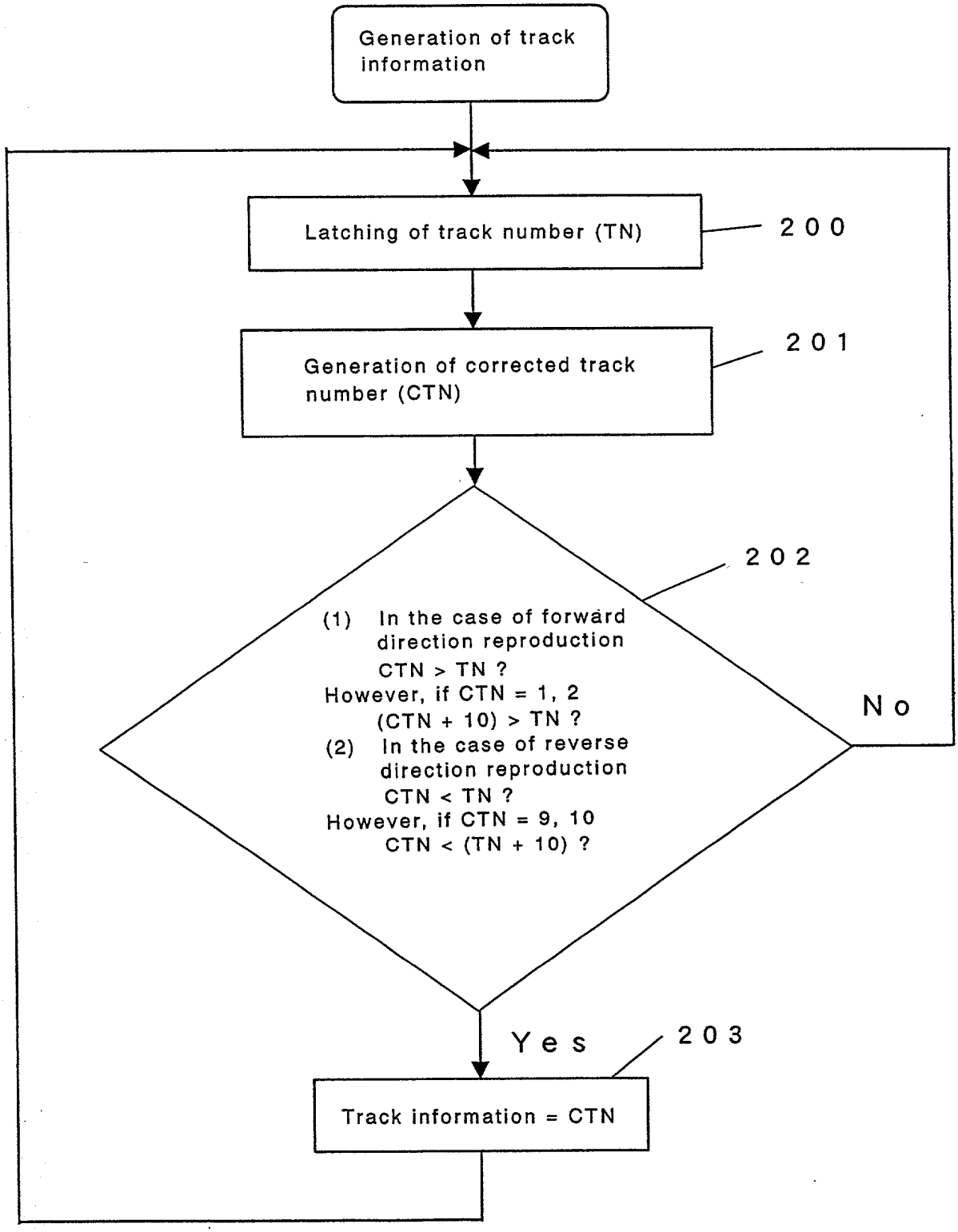

Generation of track information
Latching of track number (TN)
200
Generation of corrected track number (CTN)
201
202
(1) In the case of forward direction reproduction
CTN > TN ?
However, if CTN = 1, 2
(CTN + 10) > TN ?
(2) In the case of reverse direction reproduction
CTN < TN ?
However, if CTN = 9, 10
CTN < (TN + 10) ?
No
Yes
203
Track information = CTN

Fig. 3

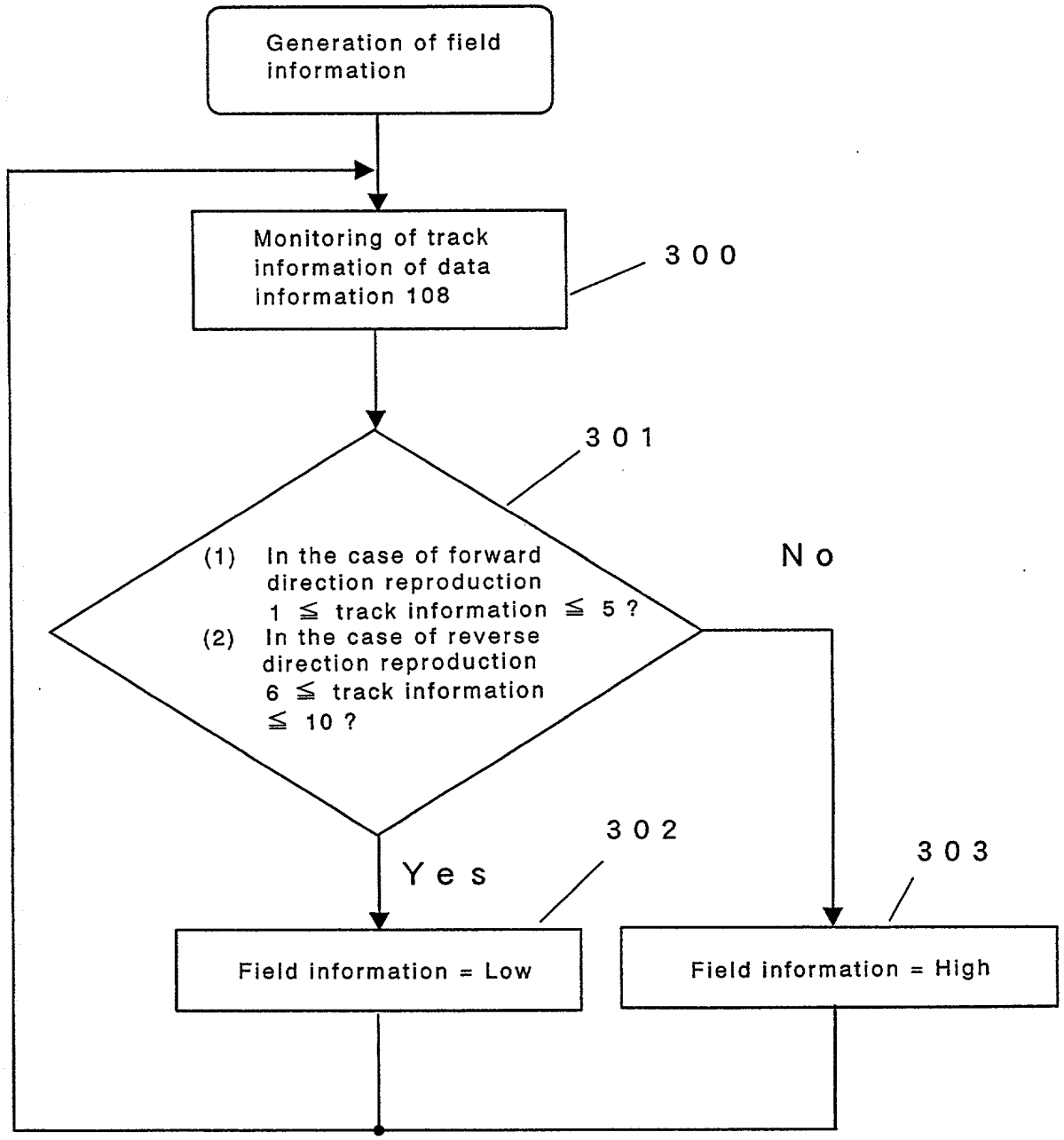

Generation of field information
Monitoring of track information of data information 108
300
301
(1) In the case of forward direction reproduction 1 ≦ track information ≦ 5 ?
(2) In the case of reverse direction reproduction 6 ≦ track information ≦ 10 ?
No
Yes
302
303
Field information = Low
Field information = High

Fig. 4

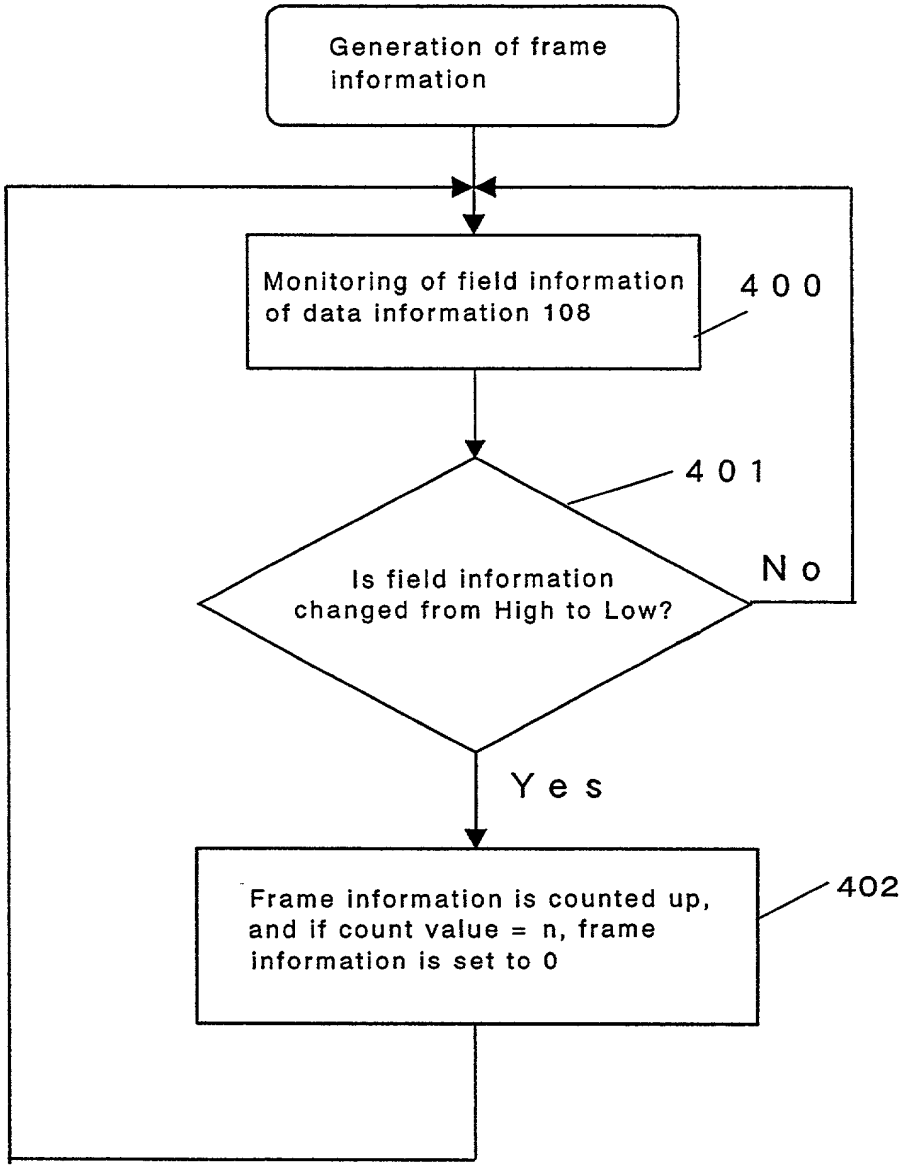

Generation of frame information
Monitoring of field information of data information 108
400
401
Is field information changed from High to Low?
No
Yes
Frame information is counted up, and if count value = n, frame information is set to 0
402

Fig. 5

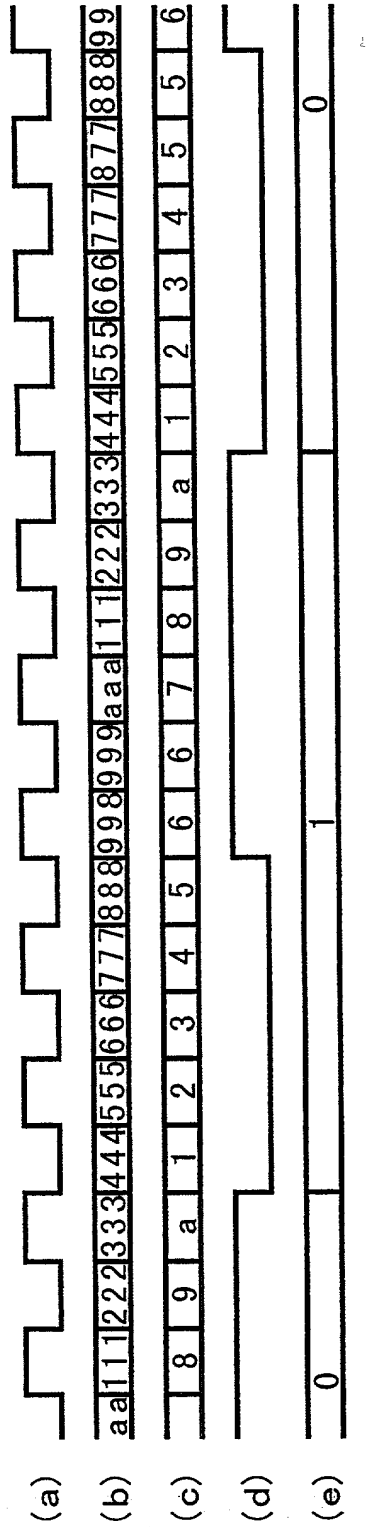


Fig. 6

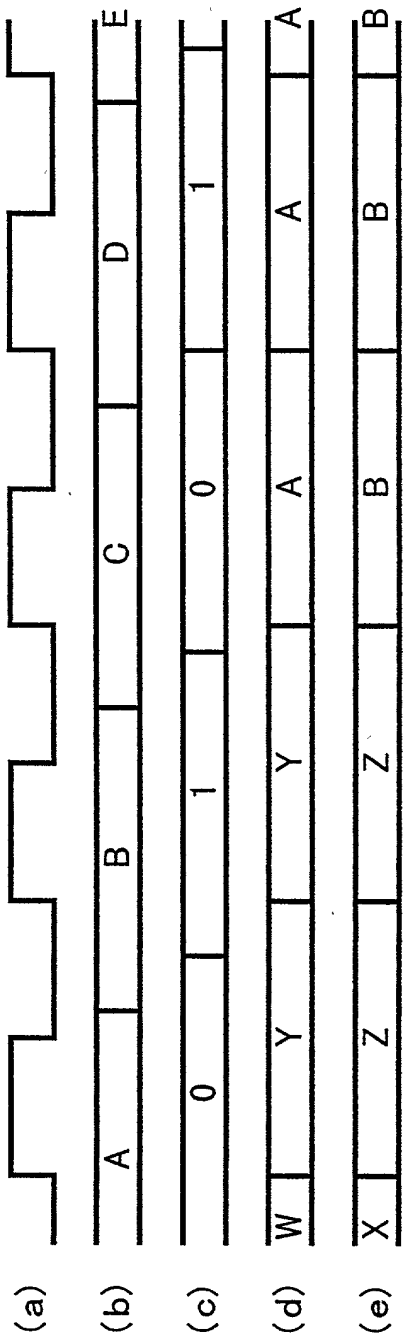


Fig. 7

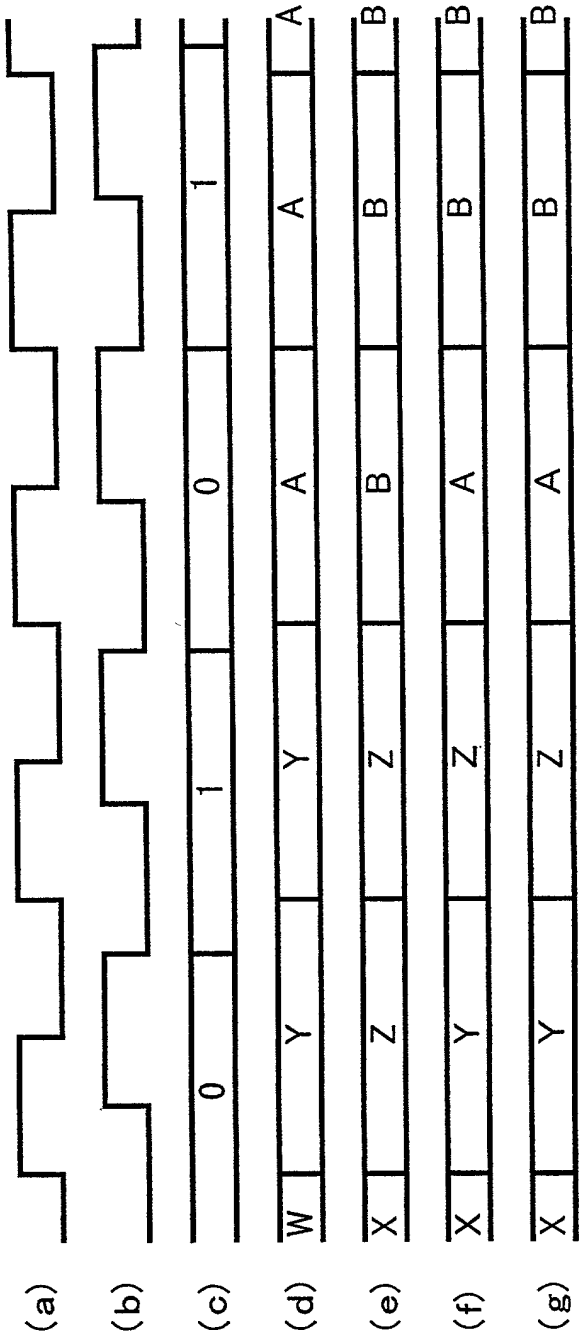


Fig. 8

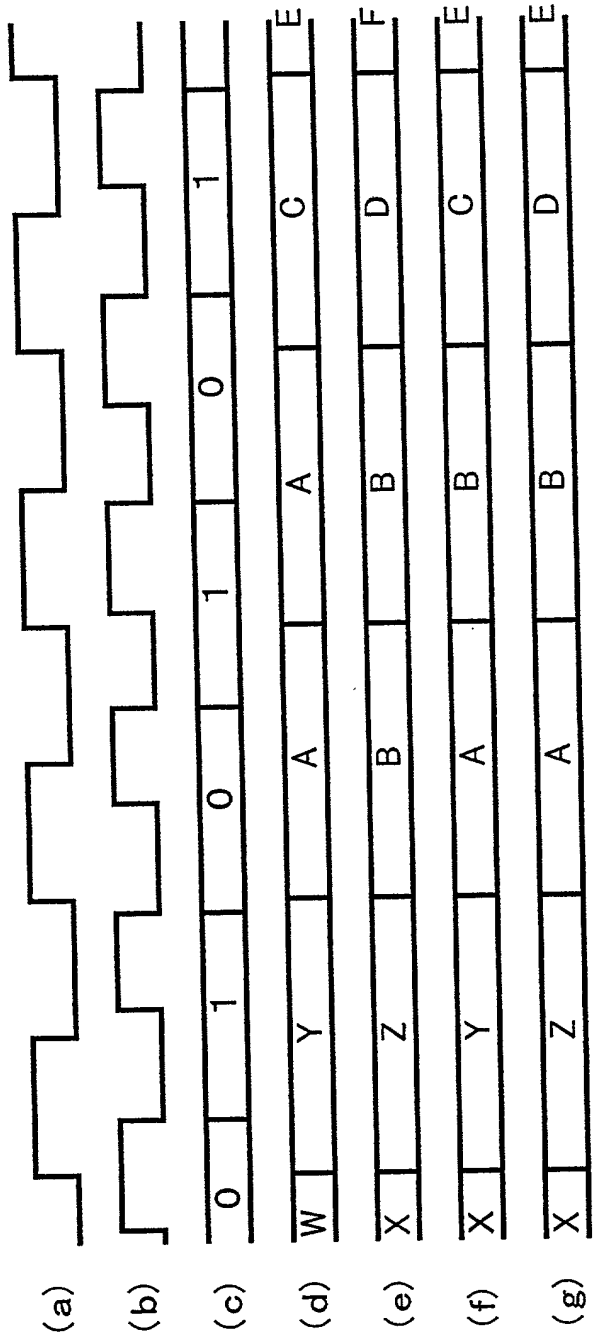


Fig. 9

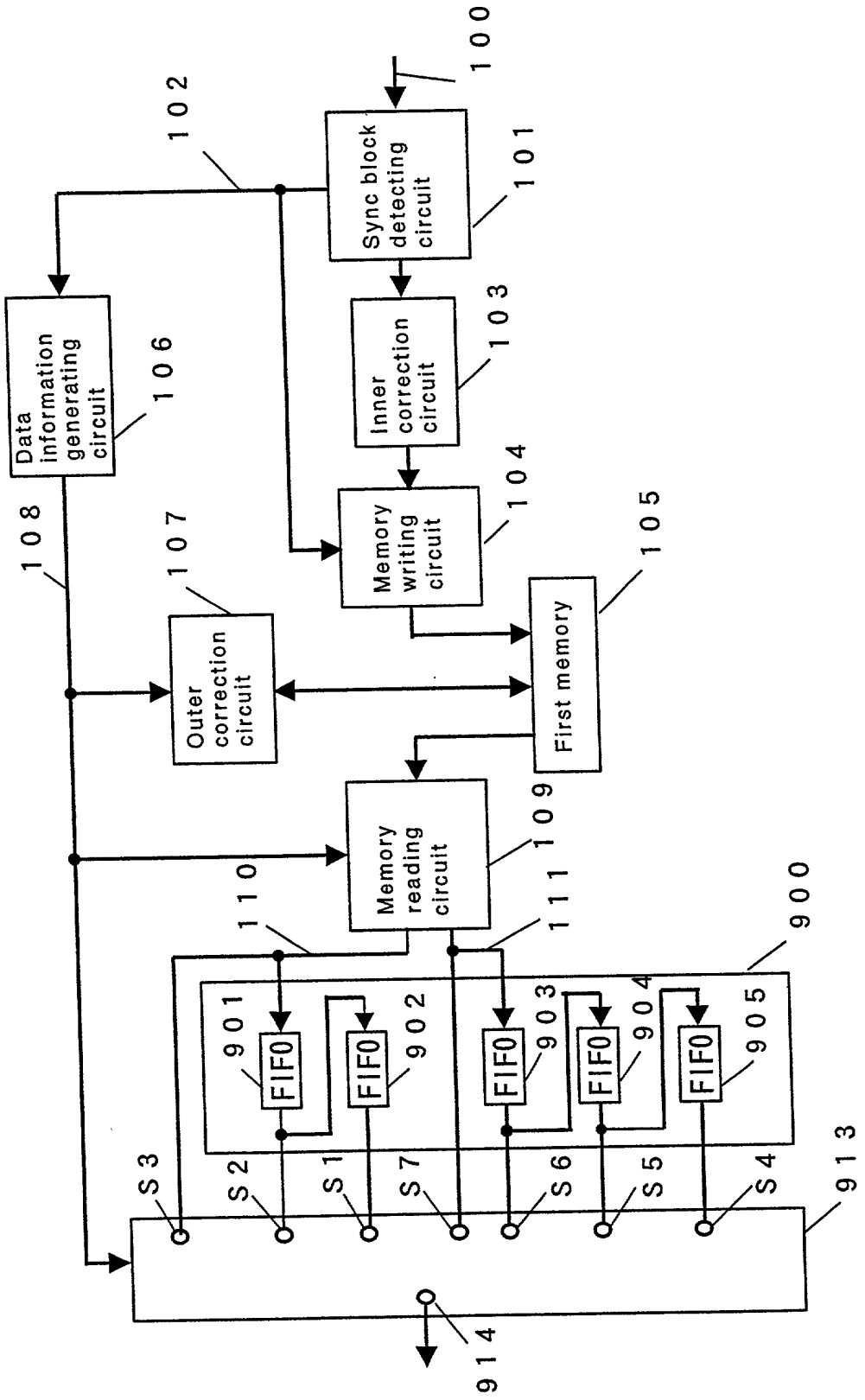

100
102
Sync block detecting circuit
101
Data information generating circuit
106
Inner correction circuit
103
Memory writing circuit
104
108
107
Outer correction circuit
First memory
105
Memory reading circuit
109
110
111
900
901
FIFO
902
903
904
905
S3
S2
S1
S7
S6
S5
S4
913
914

Fig. 10

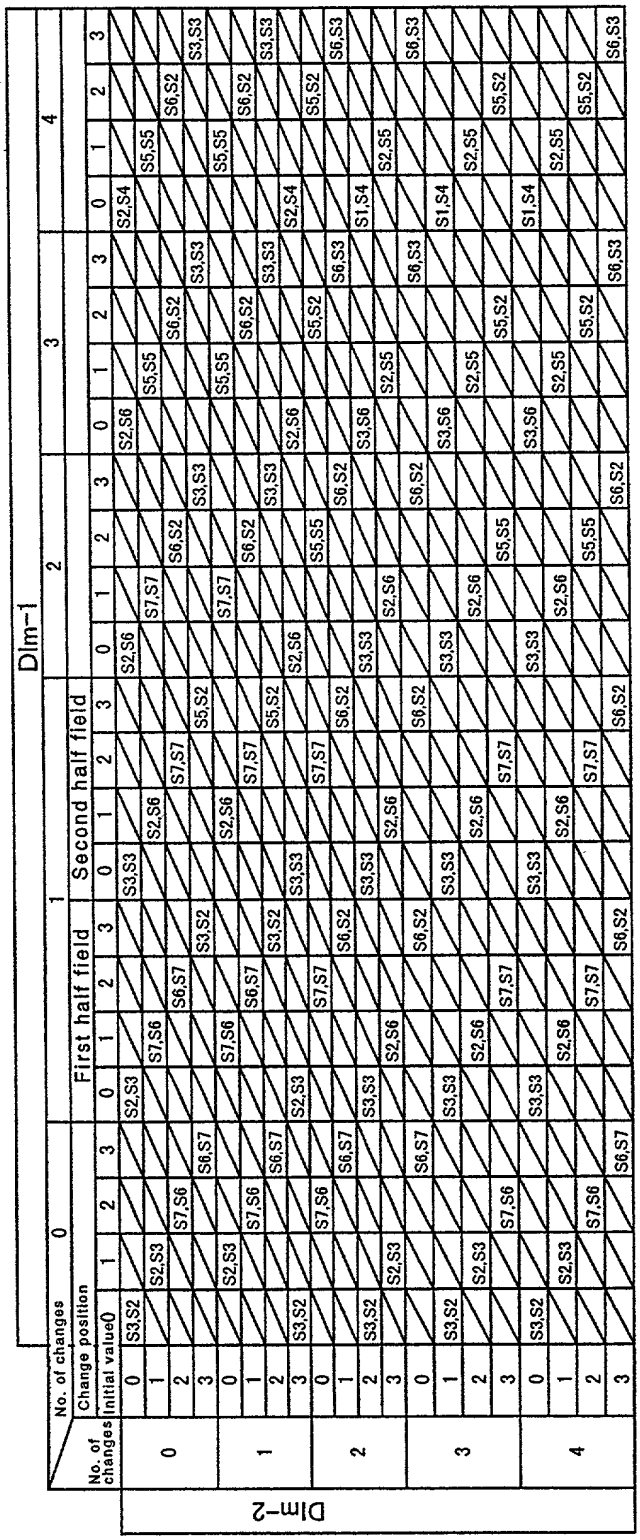

Dim-2
Dim-1
No. of changes
Change position
Initial value0
First half field
Second half field

Fig. 11

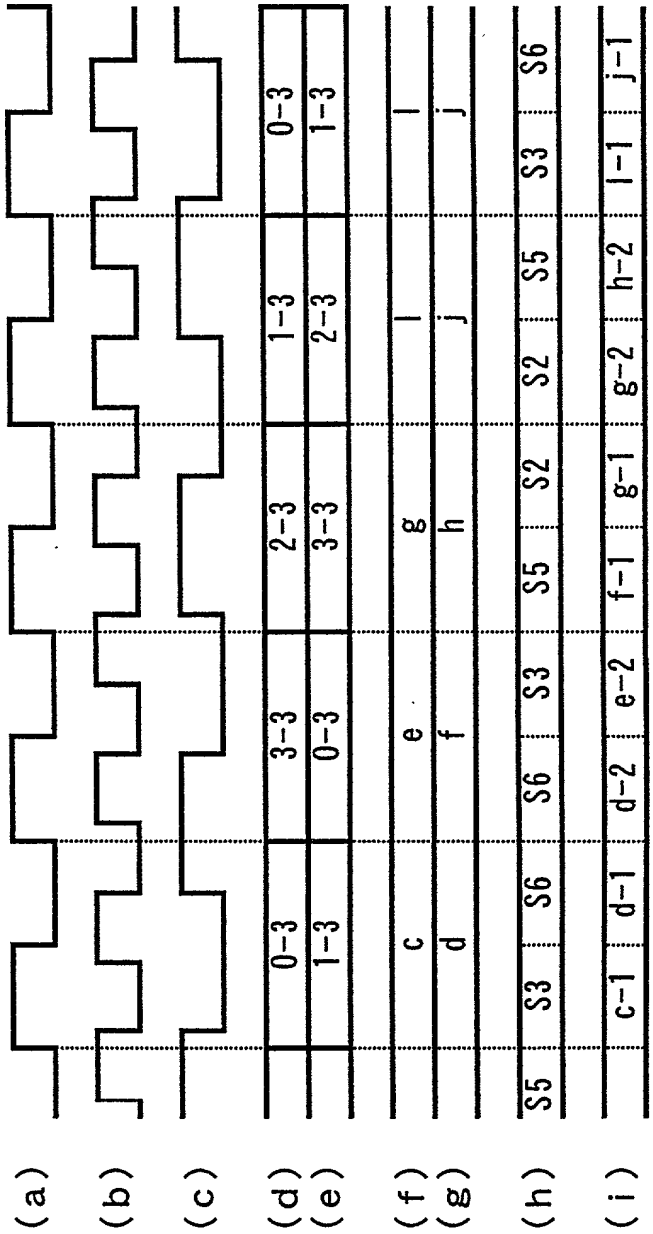

(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
S5 S3 S6 S6 S3 S5 S2 S2 S5 S3 S6
c-1 d-1 d-2 e-2 f-1 g-1 g-2 h-2 l-1 j-1
0-3 1-3 3-3 0-3 2-3 3-3 1-3 2-3 0-3 1-3
c e g l
d f h j
l
j

Fig. 12

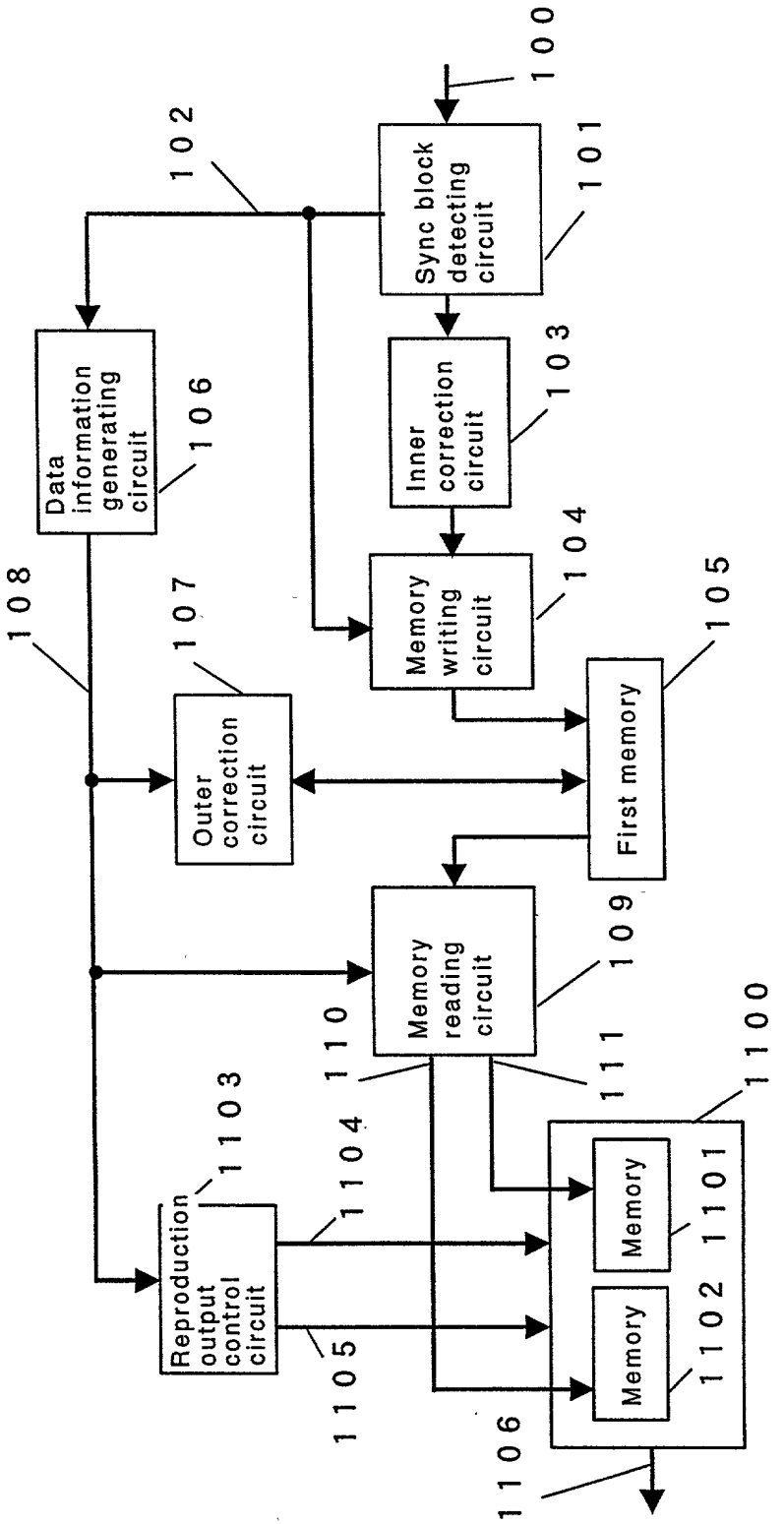

100
Sync block detecting circuit
101
102
Inner correction circuit
103
Memory writing circuit
104
First memory
105
Data information generating circuit
106
Outer correction circuit
107
108
Memory reading circuit
109
110
111
1100
Memory
1101
Memory
1102
Reproduction output control circuit
1103
1104
1105
1106

Fig. 13

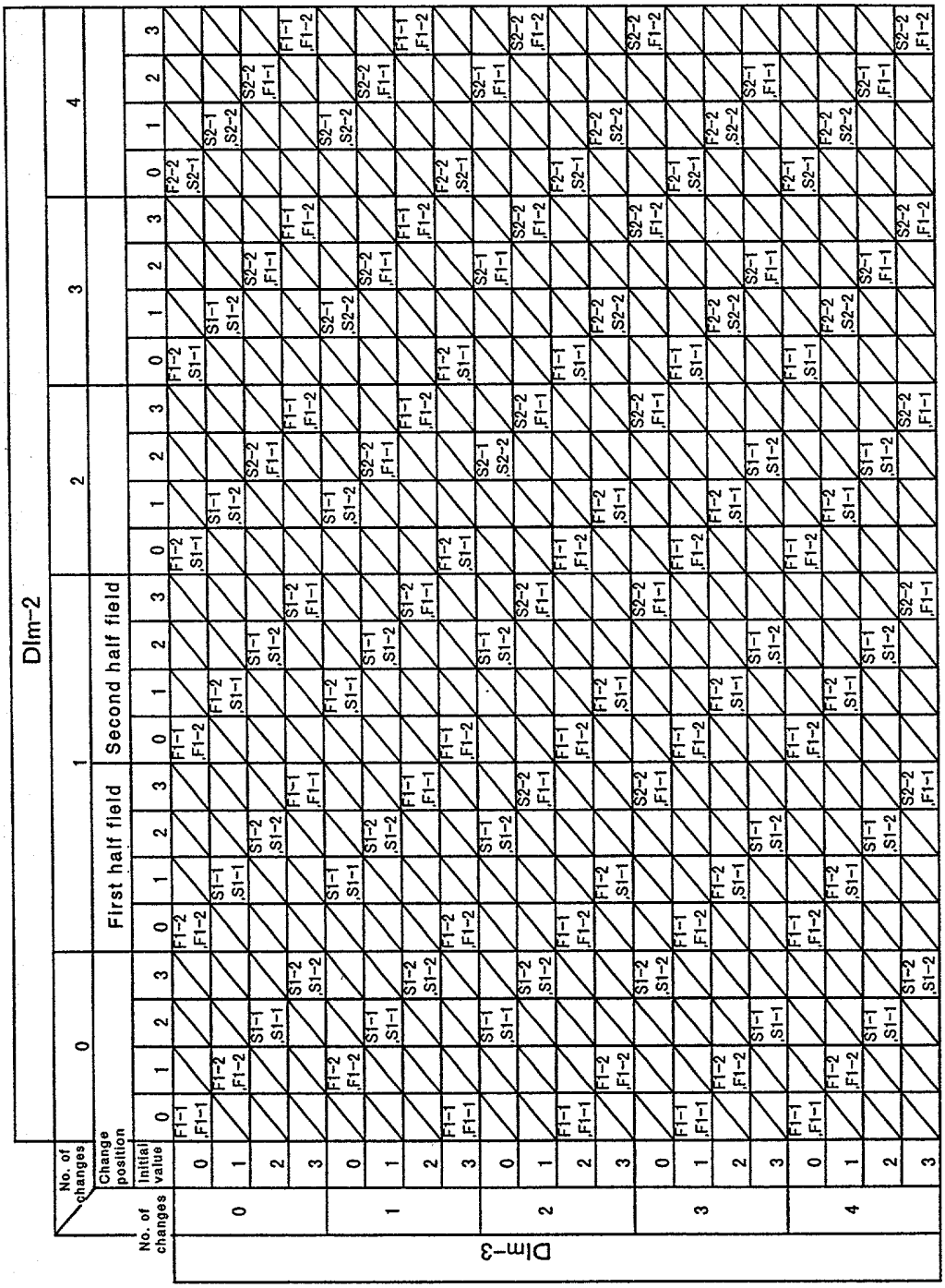

Dim-2
Dim-3
No. of changes
Change position
Initial value
First half field
Second half field

Fig. 14

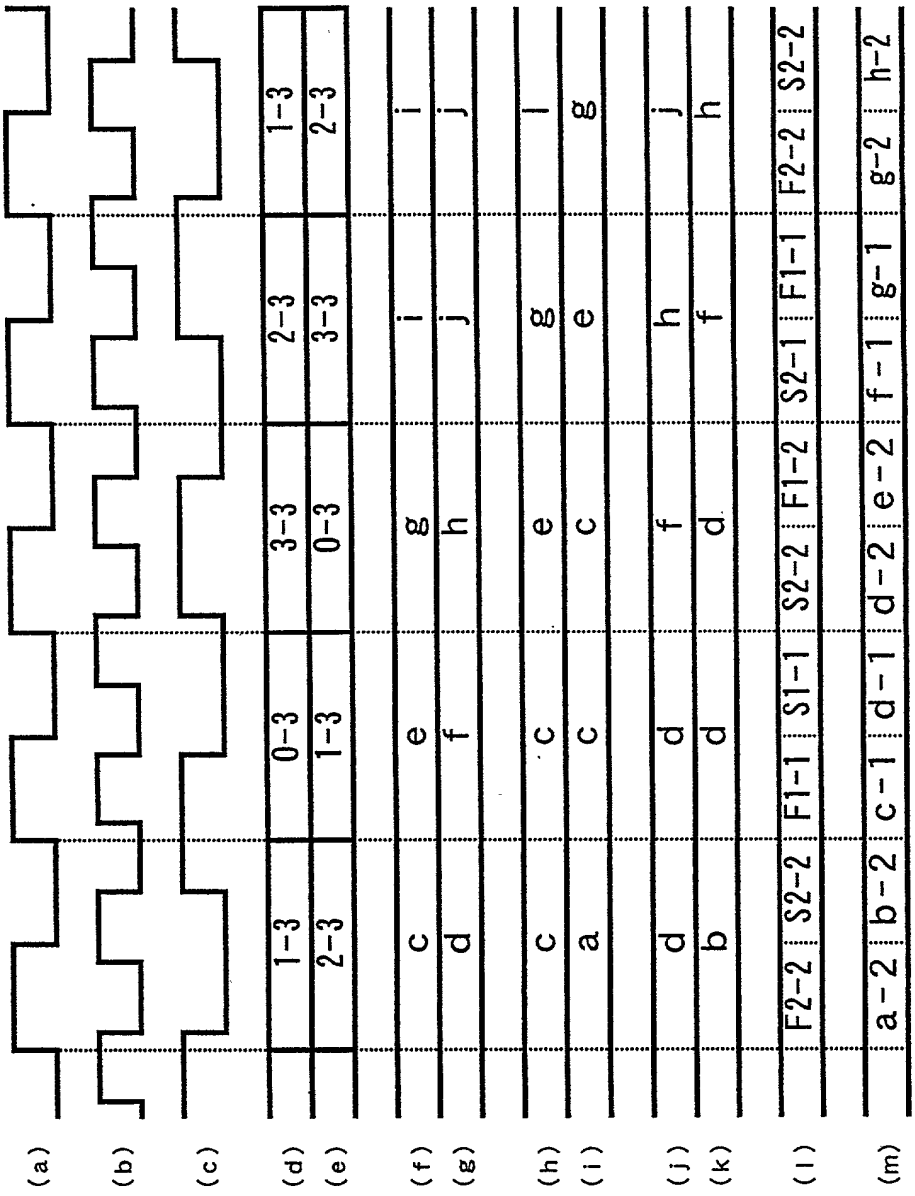

(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
(j)
(k)
(l)
(m)
1-3
2-3
0-3
1-3
3-3
0-3
2-3
3-3
1-3
2-3
c
d
e
f
g
h
i
j
c
a
e
c
g
c
l
d
b
d
d
f
h
h
j
F2-2
S2-2
F1-1
S1-1
S2-2
F1-2
S2-1
F1-1
F2-2
S2-2
a-2
b-2
c-1
d-1
d-2
e-2
f-1
g-1
g-2
h-2

Fig. 15

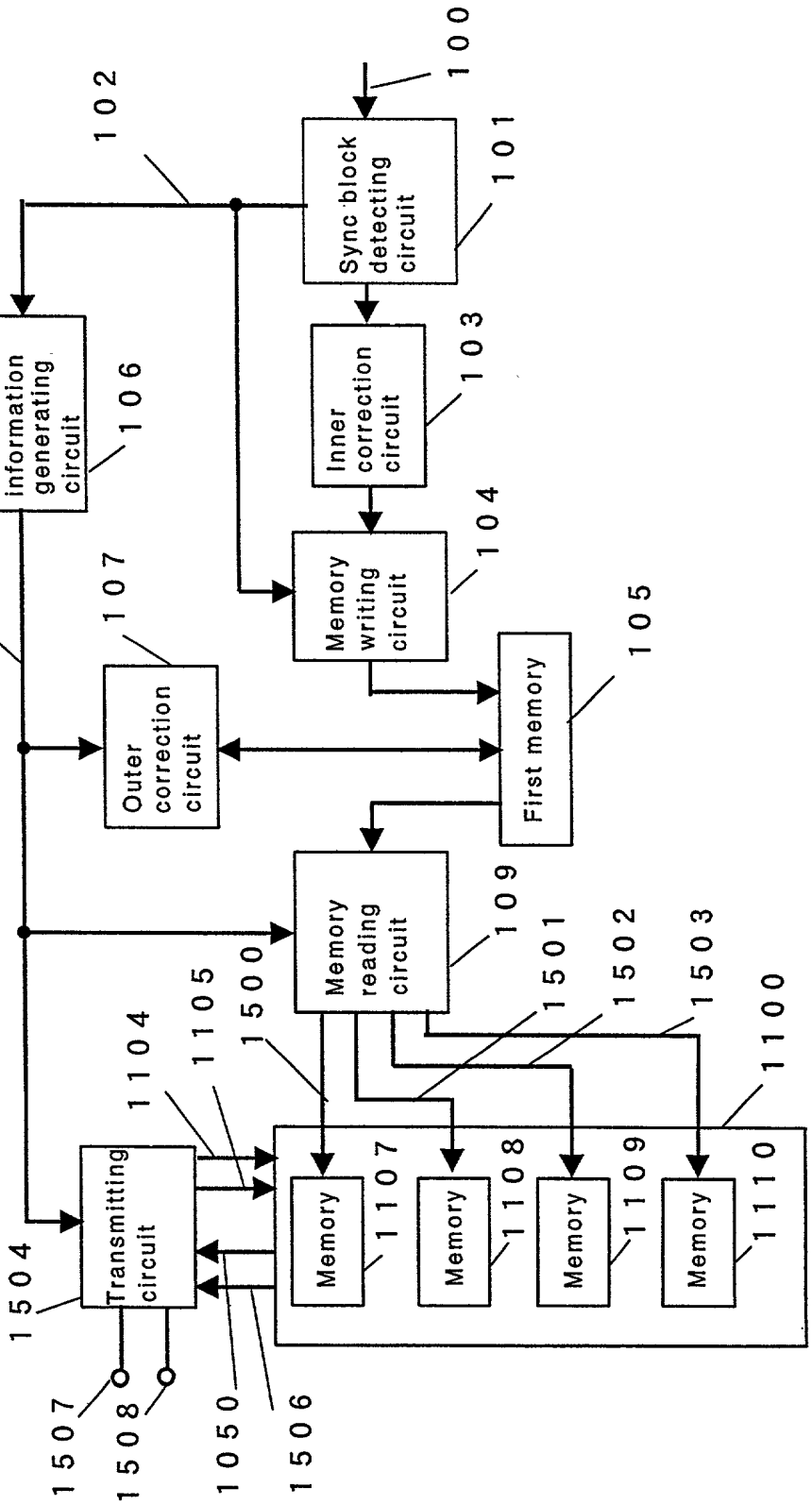
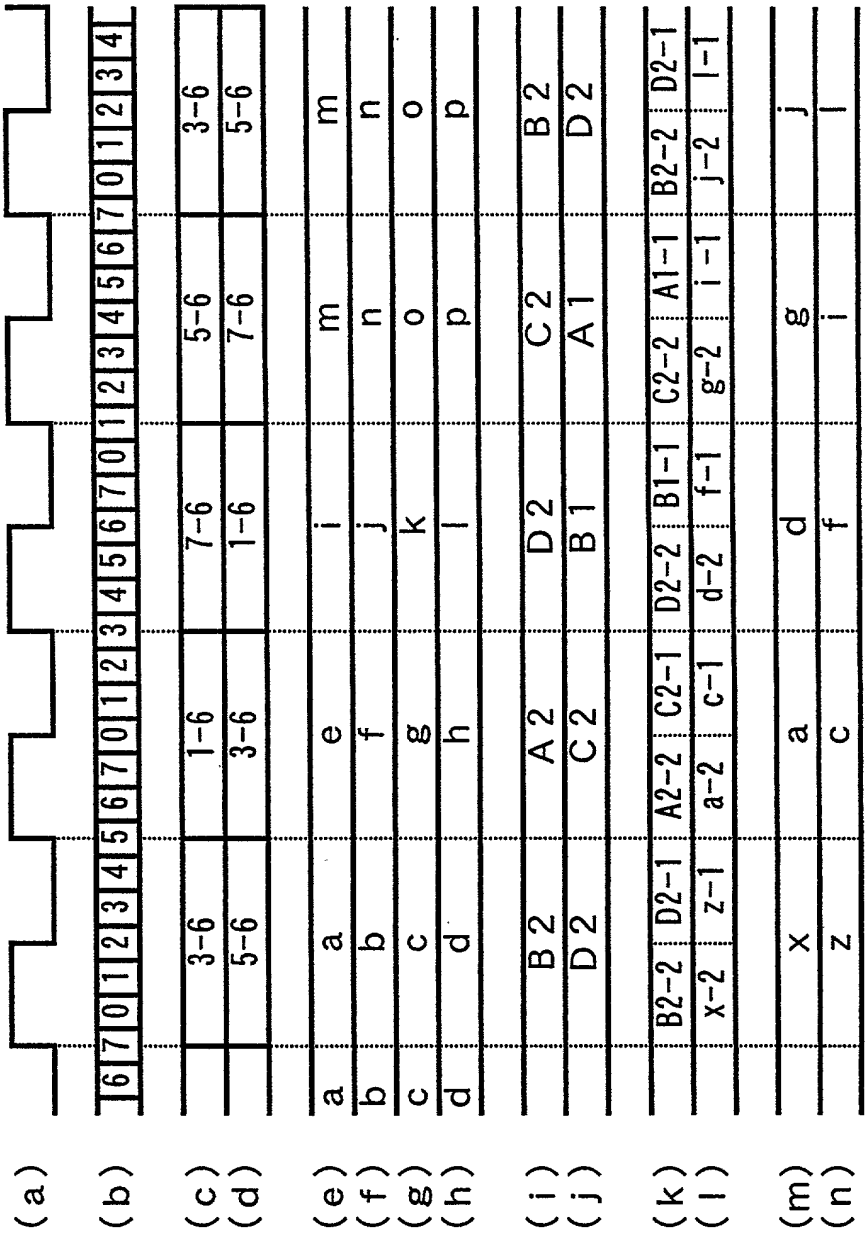

100
102
Sync block detecting circuit
101
Data information generating circuit
106
Inner correction circuit
103
Memory writing circuit
104
108
107
Outer correction circuit
First memory
105
Memory reading circuit
109
1500
1501
1502
1503
1105
1104
1100
Transmitting circuit
Memory
1107
Memory
1108
Memory
1109
Memory
1110
1504
1507
1508
1050
1506

Fig. 16


(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
(j)
(k)
(l)
(m)
(n)
6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4
3-6 1-6 7-6 5-6 3-6
5-6 3-6 1-6 7-6 5-6
a a e i m m
b b f j n n
c c g k o o
d d h l p p
B2 A2 D2 C2 B2
D2 C2 B1 A1 D2
B2-2 D2-1 A2-2 C2-1 D2-2 B1-1 C2-2 A1-1 B2-2 D2-1
x-2 z-1 a-2 c-1 d-2 f-1 g-2 i-1 j-2 l-1
x a d g j
z c f i l

LIST OF REFERENCE NUMERALS

101	Sync block detecting circuit (sync block detecting means)
104	Memory writing circuit (memory writing means)
105	First memory (first memory means)
106	Data information generating circuit (data information generating means)
109	Memory reading circuit (memory reading means)
112	Transmitting circuit (transmitting means)
900	Delay circuit (delay means)
913	Reproduction output control circuit (Reproduction output control means)
1100	Second memory (second memory means)
1103	Reproduction output control circuit (reproduction output control means)
1504	Transmitting circuit (transmitting means)

Declaration and Power of Attorney For Patent Application
English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled REPRODUCED SIGNAL PROCESSOR, the specification of which is attached hereto unless the following box is checked:

☒ was filed on July 6, 2000 as
United States Application Number or PCT International Application Number PCT/JP00/04476
and was amended on March 6, 2001 (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
11-192764	Japan	7 July 1999	☐
(Number)	(Country)	(Day/Month/Year Filed)	
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

—	—
(Application Number)	(Filing Date)
—	—
(Application Number)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

___ (Application Number)	___ (Filing Date)	___ (Status - patented, pending, abandoned)
___ (Application Number)	___ (Filing Date)	___ (Status - patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Paul F. Prestia	Reg. No. 23,031	Lawrence E. Ashery	Reg. No. 34,515	Mark J. Marcelli	Reg. No. 36,593
Allan Ratner	Reg. No. 19,717	Christopher R. Lewis	Reg. No. 36,201	Jack J. Jankovitz	Reg. No. 42,690
Andrew L. Ney	Reg. No. 20,300	Robert L. Andersen	Reg. No. 25,771	Jonathan H. Spadt	Reg. No. 45,122
Kenneth N. Nigon	Reg. No. 31,549	Joshua L. Cohen	Reg. No. 38,040	Christopher I. Halliday	Reg. No. 42,621
Kevin R. Casey	Reg. No. 32,117	Daniel N. Calder	Reg. No. 27,424	Scott A. Mckeown	Reg. No. 42,866
Benjamin E. Leace	Reg. No. 33,412	Louis W. Beardell, Jr.	Reg. No. 40,506		
James C. Simmons	Reg. No. 24,842	Jacques L. Etkowicz	Reg. No. 41,738		

Address all correspondence to: Lawrence E. Ashery
Ratner & Prestia, Suite 301, One Westlakes, Berwyn, P.O. Box 980, Valley Forge, PA 19482-0980
Address all telephone calls to: Lawrence E. Ashery at (610) 407-0700.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name) **Masatoshi Taniguchi**

100

Inventor's signature Masatoshi Taniguchi Date April 23, 2001
Residence Osaka, Japan JPX
Citizenship Japanese
Post Office Address 3-23-A-104, Higashitoyonaka-cho, Toyonaka-shi, Osaka 560-0003, Japan

Full name of second joint inventor, if any (given name, family name) **Takeshi Otsuka**

200

Second Inventor's signature Takeshi Otsuka Date April 23, 2001
Residence Osaka, Japan JPX
Citizenship Japanese
Post Office Address 4-10-11, Nishiawaji, Higashiyodogawa-ku, Osaka-shi, Osaka 533-0031, Japan

☒ Additional inventors are being named on separately numbered sheets attached hereto.

Full name of third joint inventor, if any (given name, family name) **Nobukatsu Okuda**

Third inventor's signature Nobukatsu Okuda Date April 23, 2001

Residence Osaka, Japan JPX

Citizenship Japanese

Post Office Address 6-10-10-1001, Niwajihonmachi, Neyagawa-shi, Osaka 572-0076, Japan

Full name of fourth joint inventor, if any (given name, family name) **Hirofumi Uchida**

Fourth inventor's signature Hirofumi Uchida Date April 23, 2001

Residence Osaka, Japan JPX

Citizenship Japanese

Post Office Address 4-9-83-106, Miigaoka, Neyagawa-shi, Osaka 572-0013, Japan

Full name of fifth joint inventor, if any (given name, family name) **Shinya Tanaka**

Fourth inventor's signature Shinya Tanaka Date April 23, 2001

Residence Osaka, Japan JPX

Citizenship Japanese

Post Office Address 6-Higashi 1-1206, Sotojima-cho, Moriguchi-shi, Osaka 570-0096, Japan

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